24327

B.Tech 6th Semester (ECE) F-Scheme
Examination, May–2017

VLSI DESIGN

Paper-EE-306-F

Time allowed : 3 hours] *[Maximum marks : 100*

Note : *(i) The students have to attempt **Question No.1 compulsorily** and **one** question from each section.*

*(ii) So attempt total **5** questions out of 9 questions.*

1. (i) Differentiate between Dept type MOSFET and enhancement type MOSFET. 5

(ii) Draw the stick diagram and physical design of C MoS Inverter. 5

(iii) What do you mean by Tally Ckt ? Explain AOI logic. 5

(iv) Explain the DE-MUX in detail. 5

Section-A

2. What are the advantages of IC's over discrete Ckts. Also discuss N-well process for C MoS Fabrication. 20

3. Design the N-MoS design equations in all regions. 20

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Section-B

4. Draw stick diagram and layout for the two-input C MoS NAND and NoR gate ? 20

5. Realize the following function using C MoS logic gate circuit :

   (i) Inverter

   (ii) $Y = \overline{(AB)(CD)}$

   (iii) Y = AB CD 20

Section-C

6. Discuss dynamic power dissipation and static power dissipation for C MoS. 20

7. Discuss the problem of latch up in C MoS and B1 C MoS Ckt. How it is removed ? Also explain concept of C MoS gate transistor sizing. 20

Section-D

8. Write short notes : 20

   (i) N-MoS PLA and PAL

   (ii) F PGA

9. Explain the following : 20

   (i) Test benches (counter, flip flops, FSM)

   (ii) Packages

   (iii) MUX / DEMUX

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