

Roll No.

22148

**M. Tech 2nd Semester (E.C.E)
Examination – May, 2018**

ELECTRONICS SYSTEM DESIGN

Paper : MEEC-502

Time : Three Hours] [Maximum Marks : 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

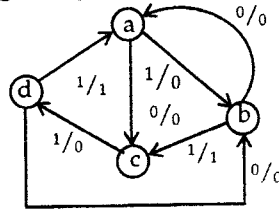
Note : Attempt any *five* question. All questions carry equal marks.

1. (a) Design and implement half adder using NAND gates. 10
- (b) Simplify the following using K-map
$$F(A,B,C,D,E) = CDE + A \bar{B} \bar{C} \bar{E} + \bar{A} B \bar{D} E + ABCE$$
2. (a) What is the need of a Comparater? Design a *two* bit comparator. 10
- (b) What is tri-state logic circuit and how does it help building a tri state bus system. 10
3. (a) Explain the design step for synchronous sequential machines. 10

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- (b) Design a circuit to convert D flip-flop to JK flip-flop. 10
4. (a) Design a circuit that will function according to the state diagram given below. Use only T flip-flop. 15



- (b) Describe why clock skew create data transmission problems. 05
5. (a) What is system controller ? Discuss the controller design phase and system documentation. 10
- (b) What is PAL ? Explain PAL based design. 10
6. (a) Discuss the timing and frequency consideration of a digital system. 10
- (b) Why shift Registers are required ? Discuss the various modes of shift register. 10
7. (a) What are essential Hazards ? How these hazards effects the operation of Machines. 10
- (b) Discuss the hazards in circuit developed by MEV method. 10
8. Write a short note on (any *two*) : 20
- (a) FPGA
- (b) Cycle and Races
- (c) Wired logic.