Roll No. .....

22151

M. E./M. Tech. 2nd Semester (ECE)

Examination – June, 2013

VLSI DESIGN

Paper : MEEC-506

Time : Three Hours] *[Maximum Marks : 100*

Before answering the question, candidates should ensure that they have been supplied the correct and complete question paper. No complain in this regard, will be entertained after examination.

Note : Attempt any *five* questions. All questions carry equal marks.

1. (a) Discuss in brief about construction and working of N-channel depletion type MOSFET. 8

(b) Discuss in brief about CMOS fabrication using : 12

(i) P-well Process,

(ii) Twin-tub Process.

2. Explain the following : 14, 6

(i) Different form of pull-up for NMOS inverter

(ii) PMOS as a switch.

3. (a) Derive an expression for pull-up to pull down ratio for NMOS inverter driving another NMOS inverter. 10

(b) Draw and discuss VTC for CMOS inverter. Also derive an expression for Noise-margin for CMOS inverter. 10

4. (a) Draw stick diagram and layout for following : 15

(i) EX-OR gate (two I/P)

(ii) AND gate using CMOS combinational logic at circuits.

(b) Write in brief about Super Buffers. 5

5. Compare the following : 7, 7, 6

(i) Constant field scaling and constant voltage scaling,

(ii) Dynamic and domino logic circuits

(iii) CMOS with B1 CMOS

6. (a) Write in detail about scaling of interconnects. 10

(b) Discuss in brief about Pseudo-NMOS inverter. 10

7. (a) Discuss in brief about design of ALU subsystem. 10

(b) Write in detail about problem of Latch-up in CMOS. Also write in detail about methods of overcoming latch-up. 10

8. Write short notes on :

(i) Carry Look Ahead Address, 10

(ii) Lambda Based Rules. 10