

Roll No. ....

**22151**

**M. Tech. 2nd Semester (E.C.E.)**

**Examination – May, 2016**

**VLSI DESIGN**

**Paper : MEEC-506**

*Time : Three Hours ]*

*[ Maximum Marks : 100*

*Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.*

*Note : Attempt any five questions. All questions carry equal marks.*

1. (a) Write in detail about construction and working of enhancement type NMOS transistor. 10
- (b) Compare NMOS and CMOS. 10
2. Draw circuit diagram and plot VTC for a NMOS inverter with : 20
- (a) Resistive load

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8. Write short notes on (any two) :  $10 \times 2 = 20$

- (b) Enhancement load
- (c) Depletion load
- (a) Write in detail about various MOS transistor parameters. 10
- (b) Draw stick diagram and layout for a CMOS inverter. 10
- Derive expression for : 20
  - (i) Noise Margin
  - (ii) Propagation delay for CMOS Inverter.
- (a) Draw and write in detail about CMOS as a switch. 10
- (b) What are domino logic circuits ? 10
- What are various scaling models ? Also discuss briefly about scaling of wires and interconnects. 20
- (a) Discuss the following for MOS devices : 14
  - (i) Short Channel Effects
  - (ii) Narrow Channel Effects
- (b) What are clocked sequential circuits ? 6