23343

M. Tech. 2nd Semester (Embedded System and Design)

Examination, May–2015

LOW POWER VLSI DESIGN

Paper–MT-VLES-506

Time allowed : 3 hours] *[Maximum marks : 100*

***Note :** Attempt any five questions.*

1. (a) What are the basic needs for Low Power VLSI Chips ? Explain. 10

   (b) What is power dissipation in CMOS devices ? Explain in detail. 10

2. (a) What is technology scaling ? Explain the effect of technology scaling on power. 10

   (b) What is transistor sizing and gate oxide thickness ? Explain. 10

3. (a) Explain the low power design circuit of flip-flop in detail. 10

   (b) What are different types of limits used in designing of low power VLSI chips ? Explain. 10

4. (a) Discuss the state machine encoding and pre-computation logic in detail. 10

   (b) What is low power memory design used in VLSI ? Explain. 10

5. Differentiate between following : 20

   (i) Single drive Vs. distributed buffer used in VLSI.

   (ii) Zero skew Vs. tolerable skew.

6. (a) Explain the design flow used in VLSI Chips. How it will be optimized ? 10

   (b) Derive the V-I characteristics and required current equation used in MOSFET. 10

7. What is low power architecture and system ? Explain. How performance of this will be managed ? 20

8. What are the algorithm and architecture level methods ? Explain the different methodologies being used. 20