

Roll No.

23332

**M. Tech. 1st Semester (VLSI Design &
Embedded System)**

Examination – December, 2014

IC FABRICATION TECHNOLOGY

Paper : MT-VLES-501

Time : Three Hours]

[Maximum Marks : 100

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt any *five* questions. All questions carry equal marks.

1. How a single crystal silicon is grown ? Explain with suitable diagram the czochralski technique for GaAs crystal growth. 20
2. (a) Compare diffusion and ion-implantation process technology. What is channeling of ion-implantations. How it reduced ? 15
- (b) Describe the mechanism of impurity diffusion from a constant source. 5

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3. Prove that oxidation of silicon surface results in an oxide layer which is about 2.27 times the thickness of the consumed silicon. 20
4. (a) Where is the need of lithography in device fabrication process ? Write main steps required in a lithography process. 10
- (b) Explain the x-ray lithography with patterning process. 10
5. (a) Explain CVD. Discuss method of poly silicon deposition and its application for IC fabrication. 15
- (b) What is lift off technique ? Give one where it is used. 05
6. (a) Discuss the mechanism of failure in metallization. 12
- (b) Explain the term 'Electromigration'. 8
7. (a) Explain the sputtering techniques. 10
- (b) Explain the wafer cleaning processes. 10
8. Write short note on : 20
- (a) CMOS process integration
- (b) MOS process integration