7. (a) What is the purpose served by ROM in a computer ? Draw the block diagram of a 32 X 8 ROM with in enable input. How many address lines and output lines are needed ? Also show that external connections of two such ROMs in order to produce 64 X 8 ROM. 7

(b) How would you convert decimal digits represented by a 7-bit ASCII into a 4 bit BCD ? 5

(c) Differentiate between the following : 2 × 2 = 4

(i) Decoder and Encoder

(ii) Level-triggered and edge-triggered flip-flop.

UNIT – IV

8. (a) What is the dynamic RAM ? How is it different from Static RAM ? Under what circumstances each of these preferred and why ? Explain. 7

(b) What is a counter ? Show that N-bit counter connected in $N \times 2^N$ decoder is equivalent to a ring counter with 2^N flip-flop Illustrate it with N = 2. 8

9. (a) What is Multiplexer (MUX) ? How will you design a 64 × 1 MUX using 8 × 1 MUS ? Illustrate. 5

(b) What are the general characteristics of a good shift registers ? Design a 3-bit shift register and outline the procedure for serial to parallel conversion and vice-versa. 6

(c) What is a mean by IC RAM ? Provide the logic diagram of such a IC memory cell. How is it possible to construct and address a 1 KB memory using 128 X 8 bit RAM chips ? Explain. 5

Roll No. .....

67043

MCA 1st Semester Last Session Dec., 15

(With New Notes)

Examination – December, 2016

DIGITAL DESIGN

Paper : MCA-103

Time : Three Hours] *[Maximum Marks : 80*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt *five* questions in all, selecting ***one*** question from each Unit. Question No. 1 is ***compulsory***. All questions carry equal marks.

1. (a) What is De Morgan's Theorem ? 8 × 2 = 16

(b) What are Self-Complementing Codes ?

(c) What are Universal Gates ? Illustrate.

(d) What are PLAs ?

(e) What are race-conditions ?

(f) What is Modulo-10 Counter ?

(g) What are race conditions in flip-flops ?

(h) Differentiate between NMOS and PMOS logic families.

UNIT – I

2. (a) What is Booth's coding ? Perform $(-11)_{16} \times (-6)_{16}$ using this method. 5

(b) What are Error-Detecting and Error-Correcting Codes ? Illustrate the significance of each. 5

(c) What is BCD arithmetic ? Perform the following BCD operations : http://haryanapapers.com 6

(i) $(5678)_{10} + (5432)_{10}$

(ii) $(9876)_{10} - (6789)_{10}$

3. (a) Why is 2's complement preferred in binary arithmetic ? Perform following operations using 2's complement : 6

(i) $(45)_{10} + (66)_{10}$

(ii) $(43)_{10} - (96)_{10}$

(b) What are Gray Codes ? Where are these useful ? Illustrate. 4

(c) Perform the operation $(1001 \times 1101)_2 + (B1.A)_{16} - (31.5)_8 + (35.5)_{10}$ and find out the result in an Octal Number System. 6

UNIT – II

4. (a) What is K-map ? Using K-map obtain the minimal expression in SOP and POS of the following expression : 10

$$F = \sum_m (0,2,4,6,7,8,10,12,13,15)$$

Implement the same in using universal gate.

(b) Illustrate the relevance of the following terms : 6

(i) Noise Margin

(ii) Propagation delay

(iii) Fan-in and Fan-out

5. (a) What is a Logic Family ? What criteria make one logic family in differ from another ? Differentiate between TTL and CMOS Logic families. 8

(b) What do you mean by Canonical SOP and POS ? Obtain canonical SOP and POS of the following function : 8

$$F(X,Y,Z) = X + Y.Z'$$

UNIT – III

6. (a) What is a Combinational Circuit ? Design a combinational circuit that receives 2 input binary number and producers its square at the output. 8

(b) What is Master-Slave flip-flop ? Discuss its working and show how the race around condition is eliminated in this flip-flop. 7