

Roll No. ....

**97666**

**B.C.A. 2nd Semester**

**Examination-May, 2015**

**Logical Organization of Computer**

**Paper-BCA-107**

**Time : 3 hours**

**Max. Marks : 80**

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Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard will be entertained after the examination.

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**Note :** Question No. 1 is **compulsory**. Attempt remaining **four** questions selecting at least **one** question from each unit. All questions carry equal marks.

1. (a) What are flip-flop excitation tables?
- (b) What is latch? —
- (c) What is the role of serial input and serial output in shift register?

- (d) Differentiate synchronous and asynchronous sequential circuit.
- (e) Discuss different memory access methods.
- (f) What is flash memory?
- (g) What is interrupt? How interrupt is handled?
- (h) What happens when a branch instruction is encountered during the execution of a program?

### **Unit-I**

- 2. (a) Discuss the operations of S-R flip-flop.
- (b) Discuss the concept of state table and state diagram with examples.
- 3. (a) What are flip-flop excitation tables? Discuss with example.
- (b) Define edge-triggered and master-slave flip-flops with diagram.

## Unit-II

4. What is shift register? Discuss the functionality of 4-bit bidirectional shift register with diagram.
5. Differentiate the following:
  - (a) Synchronous and asynchronous binary counters
  - (b) Modulo-N and Up-Down counters

## Unit-III

6. (a) Discuss different types of semiconductor memories.
  - (b) Write notes on the following:
    - (i) Optical storage devices
    - (ii) Flash memory
7. (a) What are I/O devices? Give five examples of each.
  - (b) Discuss the concept of I/O controllers.

#### **Unit-IV**

- 8.** (a) What is I/O interface? What are the needs for I/O interface?
- (b) What is priority interrupt? Discuss methods used for establishing priorities of multiple simultaneous interrupt.
- 9.** Discuss various ways to conduct DMA transfer and operation of DMA controller along with its block diagram.
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