Roll No. .....

42003

BCA (NEP) 4 Years 1st Semester
(w.e.f. Dec.-2025)
Examination – December, 2025

COMPUTER ARCHITECTURE

Paper : 25BCA401DS02

Time : Three Hours] *[Maximum Marks : 50*

Before answering the questions, candidates should ensure that they have been supplied the correct and complete question paper. No complaint in this regard, will be entertained after examination.

Note : Attempt ***five*** questions in all, selecting ***one*** question from each Unit. Question No. **1** is ***compulsory***. All questions carry equal marks.

1. (a) What is the main purpose of a control unit in CPU ?

(b) How many address lines are needed to access 64 KB memory ?

(c) What are the advantages of using Gray codes ?

(d) How does a D flip-flop differ from a JK flip-flop ?

(e) What is the role of cache memory in the memory hierarchy ?

P. T. O.

UNIT – I

2. (a) What are the benefits of using 2's complement representation for signed numbers ?

(b) How does parity bit help in detecting errors during data transmission ?

3. (a) What are the key advantages of K-map over Boolean algebra simplification ?

(b) How does Excess-3 code make BCD addition simpler ?

UNIT – II

4. (a) What is the difference between combinational and sequential circuits with examples ?

(b) How does a 4-bit parallel-in serial-out shift register work ?

5. (a) What are the excitation tables of SR and JK flip-flops and how are they used in designing counters ?

(b) How does a ring counter differ from a Johnson counter ?

UNIT – III

6. (a) What are the different types of instruction formats and how do they affect memory utilization ?

(b) How does zero-address (stack) organization simplify subroutine handling ?

7. (a) What are the main differences between RISC and CISC architectures ?

   (b) How does register addressing mode provide faster execution than memory addressing ?

UNIT – IV

8. (a) What are the common data hazards in pipelining and how can they be resolved ?

   (b) How does associative memory (cache) improve average access time ?

9. (a) What are the different mapping techniques used in cache memory and how do they affect hit ratio ?

   (b) How does demand paging in virtual memory reduce physical memory requirements ?
